A New Manufacturing Process for Fabricating 3D Interconnects for MEMS and ICs

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Abstract

The current trend in semiconductor technology toward 3-D stacking of MEMS and IC devices provides the advantages of short interconnections, miniaturization, and compact packaging. In MEMS, the interconnection using TSV requires filling vias that are 10s of microns in diameter and 100s of microns in depth. However, fabrication of such large and high aspect ratio TSV interconnects by vias electroplating or thin film deposition is costly and technologically challenging. Similarly, future generation ICs demand for very small size (<16nm) and high aspect ratio interconnects, which are extremely challenging using conventional techniques. There is a need for the development of manufacturable and cost-effective alternative interconnect fabrication techniques. In this presentation, recent challenges in 3-D integration in MEMS and IC terms of manufacturing, scaling and yield issues are reviewed and new manufacturing methods are discussed. A new, material independent, room pressure and temperature manufacturing process for fabricating 3-D interconnects is introduced.

Short Bio: Dr. Cihan Yilmaz received his Ph.D. degree in Mechanical and Industrial Engineering at Northeastern University in 2013. His research focused on micro, nano, and molecular scale directed assembly of colloids, and cost-efficient and sustainable additive manufacturing of functional nanostructures for electronics, energy, and biomedical applications. Dr. Yilmaz has authored or coauthored 15 papers and 10 patents in the field, and presented his findings in more than 50 conferences.

Dr. Yilmaz is currently working as an Innovation Engineer at Flex Boston Innovation Center, where he will be working on developing next generation products in the areas of healthcare, electronics and energy.